

Nixie Clock Main Board

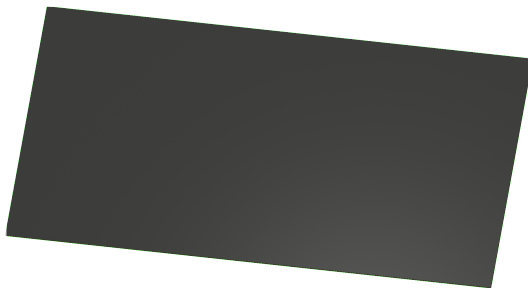
Variant: DRAFT

2026-02-28

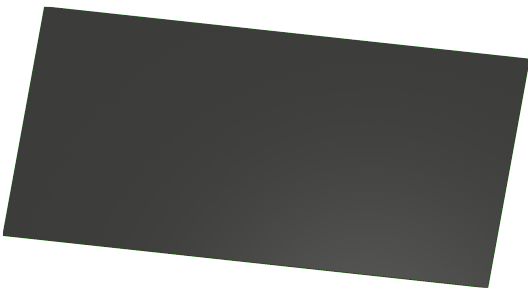
Rev + (Unreleased)

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TOP VIEW



BOTTOM VIEW



NOTES

Nixie Clock Main Board Document

Comment

Not fitted components are marked as **X**

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There shouldn't be any mistakes. Contact the engineer if you find any.

RELEASED - A board with this schematic has been sent to production.

Date: 28-Feb-2026

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for debug notes.

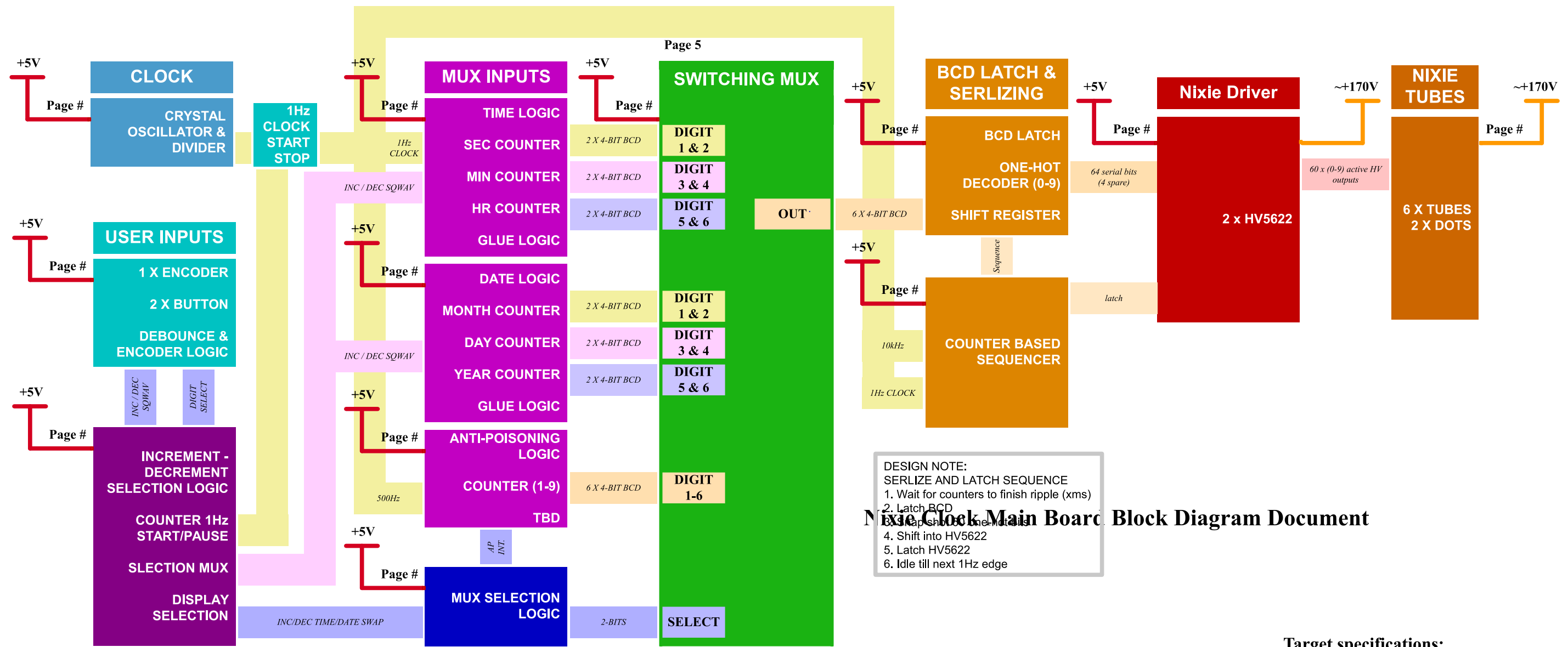
DESIGN NOTE:
Example text for cautionary design notes.

DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

	Comments:	Company: Company Name		Variant: DRAFT	
		Board Name: Nixie Clock Main Board		Project Name: Nixie Tube Clock	
	Sheet Title:	File Name: Nixie_Tube_Clock.kicad_sch	Designer: Aidan Brzezinski	Date: 2025-01-12	Revision: + (Unreleased)
	Sheet Path: /	Reviewer:		Size: A3	Sheet: 1 of 10

[2] Block Diagram



Nixie Clock Main Board Block Diagram Document

Target specifications:

Input voltage:	?? - ?? V
Spec 2	??
Spec 3	??
Spec 4	??

	Comments:	Company:		Variant:		
		Company Name		DRAFT		
		Board Name:			Project Name:	
		Nixie Clock Main Board			Nixie Tube Clock	
	Sheet Title:	File Name:	Designer:	Date:	Revision:	
Block Diagram	Block Diagram.kicad_sch	Aidan Brzezinski	2025-01-12	+ (Unreleased)		
Sheet Path:			Reviewer:	Size:	Sheet:	
/Block Diagram/				A3	2 of 10	

[3] Project Architecture

Description {

Clock - Oscillator & Divider

Page 4

File: Clock - Oscillator & Divider.kicad_sch

MUX Inputs - Time Logic

Page 5

File: Section B - Title B.kicad_sch

Switching MUX

Page 5

File: Switching MUX.kicad_sch

MUX Inputs - Date Logic

Page 5

File: MUX Inputs - Date Logic.kicad_sch

MUX Inputs - Anti-Poisoning Logic

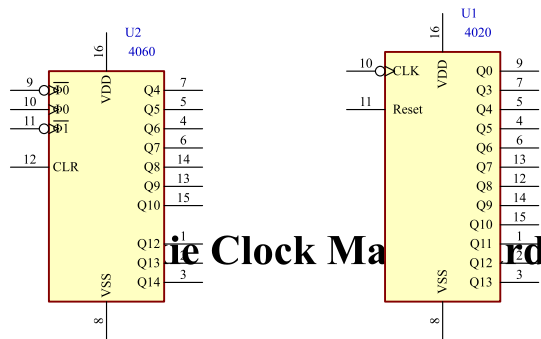
Page 5

File: MUX Inputs - Anti-Poisoning Logic.kicad_sch

Nixie Clock Main Board Project Architecture Document

	Comments:	Company:		Variant:	
		Company Name		DRAFT	
	Sheet Title:	Board Name:		Project Name:	
		Project Architecture		Nixie Clock Main Board	
	File Name:	Designer:	Date:	Revision:	
	Project Architecture.kicad_sch	Aidan Brzezinski	2025-01-12	+ (Unreleased)	
	Sheet Path:		Reviewer:	Size:	Sheet:
	/Project Architecture/			A3	3 of 10

[4] Clock



ie Clock Main Board Clock Document

Block Description

LAYOUT NOTE:
blablabla

DESIGN NOTE:
blablabla

	Comments: AN5346 STM32G474 Datasheet p.81 J. Pieper ADC investigation		Company: Company Name		Variant: DRAFT		
			Board Name: Nixie Clock Main Board		Project Name: Nixie Tube Clock		
	Sheet Title: Clock - Oscillator & Divider		File Name: Clock - Oscillator & Divider.kicad_sch		Designer: Aidan Brzezinski		
					Date: 2025-01-12		
						Revision: + (Unreleased)	
		Sheet Path: /Project Architecture/Clock - Oscillator & Divider/		Reviewer:		Size: A4	
						Sheet: 4 of 10	

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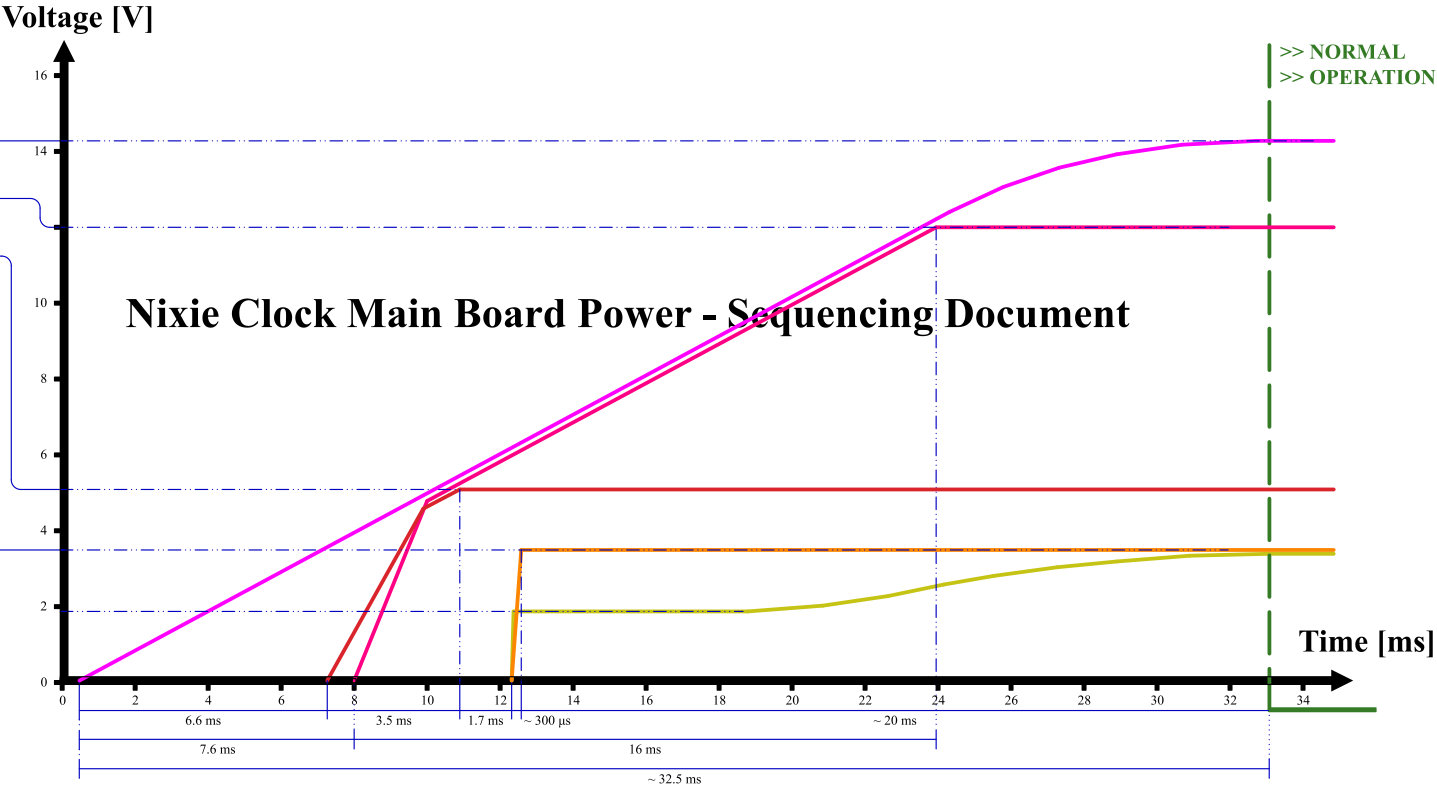
[8] Sheet Title B													
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		References:	Company Name		DRAFT		
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		Flexible I/O source configuration					
		Sheet Title:	File Name:	Designer:	Date:	Revision:	
		Switching MUX	Switching MUX.kicad_sch	Aidan Brzezinski	2025-01-12	+ (Unreleased)	
		Sheet Path:		Reviewer:		Size:	Sheet:
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[6] Power - Sequencing

NAME	SOURCE	LEVEL
+V??	??	? - ? ± ??%
+V??	??	? - ? ± ??%
+V??	??	? - ? ± ??%
+V??	??	? - ? ± ??%
+V??	??	? - ? ± ??%



	Comments:	Company:		Variant:	
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	Power - Sequencing	Power - Sequencing.kicad_sch	Aidan Brzezinski	2025-01-12	+ (Unreleased)
	Sheet Path:	Reviewer:	Size:	Sheet:	
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[7] Revision History

Nixie Clock Main Board Revision History Document

	Comments:	Company:		Variant:	
		Company Name		DRAFT	
	Sheet Title:	Board Name:		Project Name:	
		Nixie Clock Main Board		Nixie Tube Clock	
	Revision History	File Name:	Designer:	Date:	Revision:
		Revision History.kicad_sch	Aidan Brzezinski	2025-01-12	+ (Unreleased)
	Sheet Path:		Reviewer:	Size:	Sheet:
	/Revision History/			A4	7 of 10